In The Claims:

1. (original) A chip package structure comprising:

an organic substrate;

a die, wherein the die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of the die is adhered to the organic substrate; and

a thin-film circuit layer located on top of the organic substrate and the die and has an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to the corresponding metal pad of the die.

2. (original) The structure in claim 1, wherein the die has an internal circuitry and a plurality of active devices located on the active surface of the die and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry forms the metal pads.

3. (original) The structure in claim 2, wherein a signal from one of the active devices is transmitted to the external circuitry via the internal circuitry, and from the external circuitry back to one of the active devices via the internal circuitry.

4. (original) The structure in claim 3, wherein a width, length, and thickness of traces of the external circuitry are greater than corresponding traces of the internal circuitry.

5. (original) The structure in claim 1, wherein the external circuitry further comprising a power/ground bus.

6. (original) The structure in claim 1, wherein the thin-film circuit layer comprising at least a patterned wiring layer and a dielectric layer, the dielectric layer

is located on top of the organic substrate and the die, and the patterned wiring layer is located on top of the dielectric layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.

7. (original) The structure in claim 6, wherein the dielectric layer has a plurality of thru-holes, and the patterned wiring layer is electrically connected to the metal pads of the die by the thru-holes.

8. (original) The structure in claim 6, wherein a via is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die by the vias.

9. (original) The structure in claim 6, wherein the patterned wiring layer and the vias form the external circuitry.

10. (original) The structure of the claim 6, wherein the external circuitry further comprising at least one passive device.

11. (original) The structure in claim 6, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

12. (original) The structure in claim 10, wherein the passive device is formed by a part of the patterned wiring layer.

13. (original) The structure in claim 6, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

14. (original) The structure in claim 1, wherein the thin-film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in

which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin-film circuit layer and the organic substrate, the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die through the dielectric layer that is closest to the organic substrate, where the patterned wiring layer that is furthest away from the organic substrate forms the bonding pads.

15. (original) The structure in claim 14, wherein each of the dielectric layers has a plurality of thru-holes, by which each of the patterned wiring layer is electrically connected the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die through the dielectric layer.

16. (original) The structure in claim 15, wherein a via is located in each thru-hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die by the vias.

17. (original) The structure in claim 16, wherein the patterned wiring layers and the vias form the external circuitry.

18. (original) The structure in claim 14, wherein the external circuitry further comprising a passive device.

19. (original) The structure in claim 18, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

20. (original) The structure in claim 18, wherein the passive device is formed by a part of the patterned wiring layer.

21. The structure in claim 18, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

22. (original) The structure in claim 1, wherein the organic substrate further comprising an inwardly protruded area located on a surface of the organic substrate, where the backside of the die is adhered to a bottom of the inwardly protruded area.

23. (original) The structure in claim 1, wherein the organic substrate comprising an organic layer and a heat conducting layer formed overlapping, a surface of the organic substrate is a side of the heat conducting layer that is further away from the organic layer, the organic layer has at least one opening that penetrates through the organic layer used to form an inwardly protruded area, and the backside of the die is adhered to a bottom of the inwardly protruded area.

24. (original) The structure in claim 23, wherein the heat conducting layer comprising a metal.

25. (original) The structure in claim 1 further comprising a filling layer located between a surface of the organic substrate and the thin-film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.

26. (original) The structure in claim 25, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

27. (original) The structure in claim 1 further comprising a passivation layer located on top of the thin-film circuit layer and exposing the bonding pads.

28. (original) The structure in claim 1 further comprising a plurality of bonding points located on the bonding pads.

29. (original) The structure in claim 28, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

30. (original) A chip package structure comprising:

an organic substrate;

a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of each die is adhered to the organic substrate; and

a thin-film circuit layer located on top of the organic substrate and the die and has an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die and extends to a region outside the active surface of the die, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die.

31. (original) The structure in claim 30, wherein the dies perform same functions.

32. (original) The structure in claim 30, wherein the dies perform different functions.

33. (original) The structure in claim 30, wherein the dies have an internal circuitry and a plurality of active devices located on the active surface of the die, and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry forms the metal pads.

34. (original) The structure in claim 33, wherein a signal from one of the active devices is transmitted to the external circuitry via the internal circuitry, and from the external circuitry back to one of the active devices via the internal circuitry..

35. (original) The structure in claim 34, wherein a width, length, and thickness of the traces of the external circuitry are greater than corresponding traces of the internal circuitry.

36. (original) The structure in claim 30, wherein the external circuitry further comprising a power/ground bus.

37. (original) The structure in claim 30, wherein the thin-film circuit layer comprising at least a patterned wiring layer and a dielectric layer, the dielectric layer is located on top of the organic substrate and the die, and the patterned wiring layer is located on top of the dielectric layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die through the dielectric layer and forms the external circuitry and the bonding pads of the external circuitry.

38. (original) The structure in claim 37, wherein the dielectric layer has a plurality of thru-holes, and the patterned wiring layer is electrically connected to the metal pads of the die by the thru-holes.

39. (original) The structure in claim 38, wherein a via is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die by the vias.

40. (original) The structure in claim 39, wherein the patterned wiring layer and the vias form the external circuitry.

41. (original) The structure of the claim 37, wherein the external circuitry further comprising at least one passive device.

42. (original) The structure in claim 41, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

43. (original) The structure in claim 41, wherein the passive device is formed by a part of the patterned wiring layer.

44. (original) The structure in claim 37, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

45. (original) The structure in claim 30, wherein the thin-film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin-film circuit layer and the organic substrate, the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the dies through the dielectric layer that is closest to the organic substrate, where the patterned wiring layer that is furthest away from the organic substrate forms the bonding pads.

46. (original) The structure in claim 45, wherein each of the dielectric layers has a plurality of thru-holes, by which each of the patterned wiring layer is electrically connected the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the dies through the dielectric layer.

47. (original) The structure in claim 46, wherein a via is located in each thru-hole, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers, where the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die by the vias.

48. (original) The structure in claim 47, wherein the patterned wiring layers and the vias form the external circuitry.

49. (original) The structure in claim 45, wherein the external circuitry further comprising a passive device.

50. (original) The structure in claim 49, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

51. (original) The structure in claim 49, wherein the passive device is formed by a part of the patterned wiring layer.

52. (original) The structure in claim 45, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

53. (original) The structure in claim 30, wherein the organic substrate further comprising a plurality of inwardly protruded areas located on a surface of the organic substrate and the backside of the dies is adhered to a bottom of the inwardly protruded areas.

54. (original) The structure in claim 30, wherein the organic substrate comprising an organic layer and a heat conducting layer formed thereon together, a top surface of the organic substrate is a side of the heat conducting layer that is further away from the organic layer, the organic layer has a plurality of openings that

penetrate through the organic layer used to form the inwardly protruded areas, and the backside of the dies are adhered to a bottom of the inwardly protruded areas.

55. (original) The structure in claim 54, wherein the heat conducting layer comprising a metal.

56. (original) The structure in claim 30 further comprising a filling layer located between a surface of the organic substrate and the thin-film circuit layer and surrounding the peripheral of the die, and a surface of the filling layer is planar to the active surface of the die.

57. (original) The structure in claim 56, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

58. (original) The structure in claim 30 further comprising a passivation layer located on top of the thin-film circuit layer and exposing the bonding pads.

59. (original) The structure in claim 30 further comprising a plurality of bonding points located on the bonding pads.

60. (original) The structure in claim 59, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.

Claims 61 – 175 (canceled)

176. (original) A chip package structure comprising:

an organic substrate;

a die module comprising an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, whereas the backside of the die module is adhered to the organic substrate;

a filling layer located on top of the organic substrate and surrounding a peripheral of the die module, a top surface of the filling layer is planar to the active

surface of the die module;

a thin organic layer located on top of the filling layer and the die module; and

a thin-film circuit layer located on top of the thin organic layer and the die module and has an external circuitry, wherein the external circuitry is electrically connected to the metal pads of the die module and extends to a region outside the active surface of the die module, the external circuitry has a plurality of bonding pads located on a surface layer of the thin-film circuit layer and each bonding pad is electrically connected to a corresponding metal pad of the die module.

177. (original) The structure in claim 176, wherein the die module comprising a single die.

178. (original) The structure in claim 176, wherein the die module comprising a plurality of dies.

179. (original) The structure in claim 178, wherein the dies perform different functions.

180. (original) The structure in claim 176, wherein a material of the filling layer is selected from a group consisting epoxy and polymer.

181. (original) The structure in claim 176, wherein a thickness of the thin organic layer is in a range from about 2 microns to 200 microns.

182. (original) The structure in claim 176, wherein the die module has an internal circuitry and a plurality of active devices located on the active surface of the die module and the internal circuitry is electrically connected to the active devices, whereas the internal circuitry forms the metal pads.

183. (original) The structure in claim 182, wherein a signal from one of the active devices is transmitted to the external circuitry via the internal circuitry, and from the external circuitry back to one of the active devices via the internal circuitry.

184. (original) The structure in claim 183, wherein a width, length, and thickness of traces of the external circuitry are greater than corresponding traces of the internal circuitry.

185. (original) The structure in claim 176, wherein the external circuitry further comprising a power/ground bus.

186. (original) The structure in claim 176, wherein the thin-film circuit layer comprising at least a patterned wiring layer, which is located on the thin organic layer, whereas the patterned wiring layer is electrically connected to the metal pads of the die module through the thin organic layer and forms the external circuitry and the bonding pads of the external circuitry.

187. (original) The structure in claim 186, wherein the thin organic layer has a plurality of thru-holes, and the patterned wiring layer is electrically connected to the metal pads of the die module by the thru-holes.

188. (original) The structure in claim 187 wherein a via is located inside each thru-hole, and the patterned wiring layer is electrically connected to the metal pads of the die module by the vias.

189. (original) The structure in claim 188, wherein the patterned wiring layer and the vias form the external circuitry.

190. (original) The structure of the claim 186, wherein the external circuitry further comprising at least one passive device.

191. (original) The structure in claim 190, wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

192. (original) The structure in claim 190, wherein the passive device is formed by a part of the patterned wiring layer.

193. (original) The structure in claim 176, wherein the thin-film circuit layer comprising a plurality of patterned wiring layers and a plurality of dielectric layers, in which the patterned wiring layers and dielectric layers are alternately formed and the patterned wiring layers are electrically connected to the neighboring patterned wiring layers through the dielectric layer, one of the dielectric layers is formed between the thin-film circuit layer and the organic substrate, the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die module through the dielectric layer that is closest to the organic substrate, where the patterned wiring layer that is furthest away from the organic substrate forms the bonding pads.

194. (original) The structure in claim 193, wherein the thin organic layer has a plurality of first thru-holes, by which the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die module, and each dielectric layer has a plurality of second thru-holes, by which the patterned wiring layers are electrically connected to the neighboring patterned wiring layers.

195. (original) The structure in claim 194, wherein a first via is located inside each first thru-hole and a second via is located inside each second thru-hole, and each patterned wiring layer is electrically connected to the neighboring patterned wiring layers by the second vias, wherein the patterned wiring layer that is closest to the organic substrate is electrically connected to the metal pads of the die module by the first vias.

196. (original) The structure in claim 195, wherein the patterned wiring layers, the first vias, and the second vias form the external circuitry.

197. (original) The structure in claim 193, wherein the external circuitry further comprising a passive device.

198. (original) The structure in claim 197 wherein the passive device is selected from a group consisting of a resistor, an inductor, a capacitor, a wave-guide, a filter, and a micro electronic mechanical sensor (MEMS).

199. (original) The structure in claim 193, wherein the passive device is formed by a part of the patterned wiring layer.

200. (original) The structure in claim 193, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

201. (original) The structure in claim 176 further comprising a patterned passivation layer located on top of the thin-film circuit layer and exposing the bonding pads.

202. (original) The structure in claim 176 further comprising a plurality of bonding points located on the bonding pads.

203. (original) The structure in claim 202, wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.